REMARKS

The Examiner's final Office Action dated December 26, 2003 has been received and its contents carefully noted. Applicants respectfully submit that this response is timely filed and is fully responsive to the Office Action. Applicants note with appreciation the indication of allowable subject matter with regard to claims 10-18. In the present invention, claims 1-3, 10-12, 14, 17 and 18 are amended and claims 19-21 have been added. By the foregoing amendment, claims 1-21 are pending, and are believed to be in condition for allowance for at least the following reasons.

On page 2 of the Office Action, the formality rejection of the claims 1-18, under 35 U.S.C. 112 (second paragraph), has been maintained with regard to three issues. Initially, the Examiner indicates that it is not clear what is meant by "a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region" as recited in claims 1, 2, 10 and 11. Also, the Examiner indicates that it is not clear what is meant by "a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region" as recited in claims 3 and 12.

In response, Applicants again direct the Examiner to the instant specification at paragraphs [0028]-[0030] and [0040]-[0042], as well as Figure 1A and 2A, which clearly show that the storage capacitor is formed from several constituents of the pixel matrix circuit. Moreover, in the instant specification at paragraph [0105] is a description indicating that the channel formation regions or the low concentration impurity regions are formed of the same semiconductor layer as the semiconductor region that functions as an electrode of the storage capacitor. As previously stated, the storage capacitor is formed by the capacitor wiring line 203 (which is at the same device level as the first wiring layer 202a, 202b, 202c), a semiconductor region 210 (namely, a portion extended from the drain region 207, the channel region 209 and the low concentration regions 208b, 208d) and a part of the first insulating layer 204 employed as a dielectric.

As generally discussed above, this aspect of the claims indicates that a semiconductor region having the same composition as the channel formation region or the low concentration impurity region is one of the constituents to be used to compose the storage capacitor. Applicants respectfully submit that these claim features clearly set forth to one of ordinary skill in the art the subject matter which the Applicants regard as their

invention based upon a reading of the specification, as proscribed in MPEP Chapter 2173.02. The Applicant's respectfully request withdrawal of the formality rejection as it relates to the above phrases.

Finally, the Examiner indicates that it is not clear what is meant by "first wiring line through an insulating layer" as recited in claims 1 and 10. By the foregoing amendment, claims 1 and 10 have been amended to recite that "the first wiring line and the capacitor wiring line are formed on the same layer." Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection.

Applicants note that the Examiner has not provided any further guidance with regard to the 112 second paragraph rejection, even after Applicants attempted to overcome the rejection in the previous response. Applicants respectfully request that, in the absence of a withdrawal of the rejection, further explanation be provided as to the concerns of the Examiner in light of the comments provided above.

With regard to the Examiner's rejections of:

> Claims 1-6, and 9, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Hirabayashi et al. ('019) and Hashimoto et al. ('303),
>
> Claim 7, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Hirabayashi et al. ('019), Hashimoto et al. ('303) and Someya et al. ('295),
>
> Claim 8, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Hirabayashi et al. ('019), Hashimoto et al. ('303) and Murade ('722),

the Applicants respectfully traverse each of these rejections.

Applicants initially assert that the basic combination of Hirabayashi et al. (hereinafter "Hirabayashi") and Hashimoto et al. does not teach that the first wiring line and the capacitor wiring line are formed on the same layer, which is recited in all independent claims of the instant application.

That is, as previously discussed, the Hirabayashi discloses that the capacitor 70 is formed by the capacitor line 3b (which include both elements 3b illustrated). One capacitor line 3b is located above the immediate capacitor electrode 1f and one capacitor line 3b is connected to the previous or subsequent pixel. The gate electrode (scanning line) 3a is at the same level as the capacitor lines 3b, but there is no disclosure that the first wiring line and the capacitor wiring line being formed on the same layer as presently claimed. In contrast to the claimed invention, the wiring lines 3a and 3b of Hirabayashi

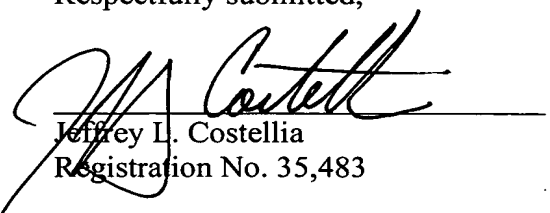
are formed above the channel region 1a (see Figure 3; paragraphs [0092]-[0096] and [0103]-[0105]).

The Examiner asserts that Hirabayashi does show such a feature. In the response to arguments section of the Office Action, the Examiner indicates that Hirabayashi does disclose that the storage capacitor is formed from a capacitor wiring line (3b) on the same layer as the first wiring layer (11a). Applicants, however, submit that the capacitor line 3b is not located on the same layer as first wiring layer 11a. As indicated in FIG. 3, element 11a is a first light shielding film which is not a wiring layer and not on the same layer as the capacitor line 3b.

Further, a review of the supporting references to Hashimoto et al., Murade and Someya reveals that none of these documents remedy the deficiency of Hirabayashi et al. by teaching a capacitor formed from a capacitor wiring line on the same layer as the first wiring layer, such that even if combined, the proposed combination would not satisfy the requirements of § 103(a) for setting forth a *prima facie* case of obviousness by teaching or suggesting each and every feature of the claimed invention. Consequently, the rejection of claims 1-18, under § 103(a) , based upon the combination of the Hirabayashi et al reference with the Hashimoto et al, Murade and Someya references, must be withdrawn.

Having responded to all objections and the rejection set forth in the outstanding Office Action, it is submitted that claims 1-18 are in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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